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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,481	04/14/2004	Vaishnav Srinivas	030333	8117

23696 7590 08/31/2005

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,481	SRINIVAS ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-12,14-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-12,14-23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner. for examination purpose only

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Amendment filed on 6/29/05 has been received and entered in the case. In view of newly discovered prior art, new ground of rejection are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted.

In view of the above noted new grounds of rejection not necessitated by Applicants Amendments, this action is non-final.

In response to Applicant's amendment filed on 6/29/05, the rejection made in the last Office action on the Shirasaki (6,587,100) and Bismarck (US Patent No. 4,450,371) are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-8, 23 and 25 rejected under 35 U.S.C. 102(b) as being anticipated by Wilford (U.S Patent No. 6,020,762).

Wilford discloses in fig. 4 a digital voltage translator including:

Regarding claim 1:

a driver (111, 113) configured to switch a current source and a current sink to a load; and

a predriver (103-109) having first and second cross-coupled inverters (cross-coupled 103-109) responsive to an input signal (102), the first inverter (109, 103) being

configured to control the switching of the current source to the load and the second inverter (105, 107) being configured to control the switching of the current sink to the load, wherein the cross-coupling between the first and the second inverters (103-109) is configured such that the first inverter (109, 103) removes the current source from the load before the second inverter (105, 107) switches the current sink to the load in response to a transition in the input signal (102), and the second inverter (105, 107) removes the current sink from the load before the first inverter switches the current source to the load in response to an opposite transition in the input signal (102), and wherein the first and second inverters (103-109) are further configured to remove both current source and the current sink from the load concurrently to allow tristate operation (111, 113, 149, 151, 153, 155) of the driver.

Regarding claim 2: each of the inverters comprises a pair of transistors connected in series (105, 107, 109, 103).

Regarding claim 3: each of the transistors comprises a field effect transistor (103-109).

Regarding claim 4: each of the inverters (103-109) comprises a p-channel FET (105, 109) having a drain and an n-channel FET (107, 103) having a drain connected to the drain of the PFET.

Regarding claim 5: each of the inverters (103-109), the NFET (107, 103) comprises a gate responsive to the input signal (102), and the PFET (i.e., 105) comprises a gate coupled to the drain of the PFET (109) in the others inverter.

Regarding claim 7: Wilford is silent in Fig. 4 about size for transistors 103-105, thus assume 105 =109 in size and 107=103 in size.

Regarding claim 8: Element VDD2 reads on a voltage source coupled to the inverters.

Regarding claim 23:

inverter means (101) for receiving an input signal and inverting the input signal (102); cross-coupled inverter means (103-109) for providing a break-before make delay, wherein the cross-coupled inverter means (103-109) is configured to receive the output of the inverter means (101), and the cross coupled inverter means is further configured to receive the output (B) of the inverter means (101), and the cross-coupled inverter means (103-109) is further configured to receive the input signal (102); and

first and second output buffer means (111. 113) for receiving first and second outputs (C, D) of the cross-coupled inverter means (103-109); and

first and second tristate means (155, 153, 151, 149) for disabling output signals of the first and second predriver output nodes.

Regarding claim 25: voltage supply means (VDD2) for supplying a higher voltage at predriver output nodes than a voltage of the input signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilford as applied to claims 1-5 above.

Although Wilford, Fig. 4 does not expressly state the size value for the transistors, this difference is not of patentable merit because it is notoriously well known in the art that different sizes for the transistors can be selected in order to produce correspondingly different output values. Clearly, if designer wish to triggering faster and improving circuit reliability, there is well-known way to do such as: increasing the size for the transistor 107/103 and decreasing the size for transistors 105 and 109 of Wilford.

Claims 10-12, 14-22 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilford.

Regarding claim 10:

an input inverter (101) configured to receive an input signal (102);

two cross-coupled inverters (103-109) that include a first and second NFET (107, 103) and a first and second PFET (105, 109), wherein the first NFET (107) is configured to receive the output of the input inverter (101), and wherein the second NFET (103) is configured to receive the input signal (102);

first and second output buffers (111, 113) configured to receive first and second outputs (C, D) of the two cross-coupled inverters (103-109);

first and second tristate devices (155, 153, 151, 149) configured to disable output signals of the first and second predriver output nodes (C, D).

However, this reference does not specifically disclose "the NFETs of the cross-coupled inverters are larger than the PFETs of the cross-coupled inverters".

The same motivation applied to claim 6 is applied to claim 10.

Regarding the limitation "are sized with respect to each other" recited in claim 11: the same motivation applied to claim 6 is applied to claim 11.

Regarding claim 12: the PFETs of the cross-coupled inverters are substantially equal in size (Wilford is silent about sizes for 105 and 109, thus, assume size of 105 = size of 109).

Regarding claim 14: each tristate device is a logic gate (155, 153 together with 111 form a NOR gate) and (151, 149 together with 113 form NAND gate), ENABLE and ENABLE* read on a disable signal.

Regarding claim 15: the first tristate device is an NAND gate (151, 149 together with 113 form NAND gate), and the second tristate device is a NOR gate (155, 153 together with 111 form a NOR gate).

Regarding claim 16: the first tristate is an NFET (149) and the second tristate device is a PFET (155).

Regarding claim 17: elements 111, 113 read on an output driver device.

Regarding claim 18: each of the input inverter (101), the cross-coupled inverters (103-109), first and second output buffers (111, 113) are capable sized so as to be sufficiently large to drive the capacitive load.

Regarding claim 19: the output driver device (111, 113) includes an NFET device (121, 127) and a PFET device (125, 119).

Regarding claim 20: element VDD2 reads on a voltage supply, element VDD1 reads on an input voltage.

Regarding claim 21: The voltage supply (VDD2) is coupled between the first and second PFETs (105. 109) of the cross-coupled inverter (103-109).

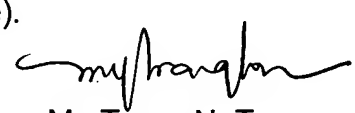
Regarding claim 22: the output buffers include one or more inverters (111, 113).

Claims 26 and 27 are similarly rejected as claims 10-11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

August 30, 2005